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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,774	12/28/2001	Michael Burrows	9772-0337-999	2125

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EXAMINER	
ROMANO, JOHN J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,774	BURROWS ET AL.	
	Examiner	Art Unit	
	John J Romano	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims **1-33** are pending in this action.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims **1 - 6, 8 - 10, 12 - 17, 19 – 21, 23, 24 – 28** and **30 - 32** are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Chase et al., US 6,149,318, (hereinafter **Chase**).

3. In regard to claim **1**, **Chase** discloses:

- "*A method of dynamically verifying program operation, comprising: executing a specified computer program...*" (E.g., see Figure 4 & Column 17, lines 10 – 26), wherein, dynamic or run-time verification of a specific program is achieved via instrumentation.
- "*...while executing the specified computer program, maintaining a shadow array, the shadow array having entries corresponding to respective memory locations used by the specified computer program, each entry of the shadow array indicating a data type of the corresponding respective memory location...*" (E.g., see Figure 4 & Column 18, lines 3 - 7), wherein, the table is the shadow array.
- "*...the execution of the specified computer program including executing each of a plurality of instructions of the computer program,*

wherein execution of each instruction of a subset of the plurality of instructions includes: determining whether execution of the instruction is inconsistent with an entry of the shadow array and generating a report when execution of the instruction is determined to be inconsistent with the entry of the shadow array; executing the instruction; and updating the shadow array in accordance with execution of the instruction." (E.g., see Fig 8 & Column 17, lines 10 – 26), wherein, the table or shadow array is maintained or updated, and referenced for consistency or inconsistency, for reporting errors or generating a report.

4. In regard to claim **2**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*identifying a memory location to be accessed by the instruction*; *inspecting the shadow array entry corresponding to the identified memory location*..." (E.g., see Figure 4 & Column 17, lines 10 – 24), wherein, the first data structure maps the location and the second maps the type and returns a Boolean indicating an error or not.

5. In regard to claim **3**, **Chase** discloses the method of claim **2** as described above and furthermore, **Chase** discloses:

- "...*comprises a read operation*..." (E.g., see Figure 4 & Column 32, lines 38 - 48), wherein, the computer reads the memory.

6. In regard to claim **4**, **Chase** discloses the method of claim **2** as described above and furthermore, **Chase** discloses:

- "...*comprises a write operation*..." (E.g., see Figure 4 & Column 32, lines 38 - 48), wherein, the computer writes to memory to operate to perform the function of maintaining the table or shadow array.

7. In regard to claim **5**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*includes determining whether proper execution of the instruction requires accessing data of a predefined data type that is different from the data type specified by the entry of the shadow array.*" (E.g., see Figure 4 & Column 17, line 51 – Column 18, line 7), wherein, a data structure would be defined and later queried to see if complete.

8. In regard to claim **6**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*is inconsistent with the data type specified*..." (E.g., see Figure 4 & Column 6, lines 14 – 19), wherein improperly corresponding or inconsistent to the common given program entity or data type specified.

9. In regard to claim **8**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*indicates whether the corresponding memory location has been allocated.*" (E.g., see Column 18, line 56 – Column 19, line 5), wherein,

the table is registered and manipulated to correspond to allocated memory.

10. In regard to claim **9**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*has been initialized.*" (E.g., see Column 20, lines 6 – 18), wherein, the table or shadow array is initialized.

11. In regard to claim **10**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*compiling a source code program into a specified computer program...*" (E.g., see Figure 4 & Column 4, lines 12 – 19), wherein, the language processor or compiler where the front end input is a source code program and the abstract syntax tree or intermediate code is the specified computer program.
- "...obtaining debugging information related to the specified computer program; and initializing the shadow memory based on the debugging information." (E.g., see Figure 18 & Column 13, lines 17 - 20), wherein, information obtained from the intermediate code is used to initialize the table or shadow memory and then validate or debug the program.

12. In regard to claim **12**, Claim **12** is a product version of claim **1** and thus, the limitations described in claim **1**, respectively correspond to claim **12**. **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*an interpreter module.*" (E.g., see Column 32, lines 36 – 37), wherein, the language may be interpreted.

13. Claims **13 - 17,** and **19 - 21** are product versions of the method claims of **2 – 6** and **8 - 10**, respectively. Thus, the limitations as described in the corresponding claims apply to and meet the limitations of claims **13 – 17** and **19 - 21.**

14. In regard to claim **23**, Claim **23** is a product version of claim **1** and thus, the limitations described in claim **1**, respectively correspond to claim **12**. **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "...*a program instrumenting module for adding dynamic checking instructions to a compiled program to generate an instrumented program...*" (E.g., see Column 2, lines 40 - 53), wherein, the program in instrumented for run-time checking or dynamic checking instructions to a compiled program to generate an instrumented program.

15. Claims **24 – 28** and **30 - 32** are product versions of the method claims of **2 – 6 and 8 - 10**, respectively. Thus, the limitations as described in the corresponding claims apply to and meet the limitations of claims **24 – 28** and **30 - 32.**

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims **7 & 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chase** in further view of Chao et al., US 5,995,752, (hereinafter **Chao**).

18. In regard to claim **7**, **Chase** discloses the method of claim **1** as described above and furthermore, **Chase** discloses:

- "... *stack locations, and memory heap locations.*" (E.g., see Figure 4 & Column 18, line 27 – Column 19, line 21), wherein, it is well known in the art that a user-controlled memory location in assembly may be a CPU register.

But **Chase** does not expressly disclose "... *CPU registers*...". However **Chao** discloses:

- "... *CPU registers*..." (E.g., see Column 3, lines 17 - 22), wherein, the CPU registers are saved in order to keep current memory status.

Chase and **Chao** are analogous art because they are both concerned with the same field of endeavor, namely, memory status operations. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to combine via assembly language CPU registers with **Chase's** invention of run-time error checking. The motivation to do so would have been to make system specific calls (E.g., see Chase Column 19, lines 13 – 14). Also, **Chase** makes reference to implementing a run-time program in "assembly language" (Column 32, line 35) which would imply using CPU registers.

19. Claims **11** & **22** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chase** in further view of Grossman et al., US 5,987,249, (hereinafter **Grossman**).

20. In regard to claim **11**, **Chase** discloses the method of claim **1** as described above. But **Chase** does not expressly disclose "...*not executing the instruction when execution of the instruction is determined to be inconsistent...*". However, **Grossman** discloses:

- "...*not executing the instruction when execution of the instruction is determined to be inconsistent...*", (E.g., see Column 18, lines 47 – 54), wherein, **Grossman** teaches stopping execution of the code in response to an error or inconsistent type.

Chase and Grossman are analogous art because they are both concerned with the same field of endeavor, namely, program instrumentation for run-time error checking. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to stop a program when finding an error in Chase' run-time error checking instrumentation. The motivation to do so would have been to stop a faulty program from running and doing more damage. Thereby, wasting further time and money.

21. In regard to claims **18** and **22**, claims **18** and **22** are product versions of claim **7** and **11**, respectively. Thus, the limitations, as described in the corresponding claims, apply to and meet the limitations of claims **18** and **22**.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **Dolin et al.**, US 6,594,783.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Romano whose telephone number is (571)-272-3872. The examiner can normally be reached on 8-5:30, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q Dam can be reached on (571)-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TUAN DAM
SUPERVISORY PATENT EXAMINER